Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 4- 6, 9-11, 14 and 15 have been amended. Claims 3, 8, and 13 have been cancelled. Claims 16-21 have been added. Claims 2, 7, and 12 were previously cancelled. Therefore, claims 1, 4-6, 9-11, and 14-21 are presented for examination.

35 U.S.C. §102(e) Rejection

Claims 1, 3-6, 8-11 and 13-15 stand rejected under 35 U.S.C. §102(e) as being clearly anticipated by Rozas et al. (U.S. Patent No. 6,725,361). Applicant submits that the present claims are patentable over Rozas.

Rozas discloses a floating point processor including a plurality of explicitly-addressable processor registers and an emulation register capable of storing a value used to logically rename the explicitly-addressable registers to emulate registers of a floating point stack. The processor further includes a computer-executable software process for calculating and changing a value in the emulation register to a value indicating a change in addresses of registers of the floating point stack when executing a floating point stack operation. The processor also includes adder circuitry combining a register address and the value of the emulation register in response to the computer-executable process to rename the plurality of explicitly-addressable processor registers. (Rozas at Abtract.)

Claim 1 recites:

> A method of translating instructions, said method comprising: translating a first block of instructions executable in a first processor architecture, into a translated first block of instructions executable in a second processor architecture, said translated first block of instructions operating with a stack of data entry positions; and

during the translating, generating an expected Top of Stack (TOS) position in said stack for said first block of instructions; and

during the translating, adding at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS position in said stack at a time of executing said translated first block of instructions;

wherein said at least one instruction branches to correction code if said expected TOS is not equal to said actual TOS, and

wherein said correction code to generate a delta of said expected TOS and said actual TOS and to adjust said stack for said first block of instructions by the delta at the time of executing said first block of instructions.

Applicant submits that Rozas does not disclose or suggest adding an instruction during translation, the instruction branches to correction code if said expected TOS is not equal to said actual TOS, and wherein said correction code to adjust said stack for said first block of instructions at the time of executing said translated first block of instructions, as recited by claim 1. The Final Office Action cites Rozas at column 10, line 66 through column 11, line 10 as disclosing "said instruction added to said first block of instruction, branches to correction code if said expected TOS is not equal to said actual TOS." (Final Office Action mailed 8/15/05 at pg. 6, point 11 referring to Office Action mailed 6/1/04 at pg. 3, point 4.).

However, this portion of Rozas actually states "the translation software rolls back execution to the beginning of translation, adjusts the host top-of-stack and current prediction so that the new current prediction is the translation-line prediction.... The translation is then restarted from the beginning" (Rozas at col. 11, ll. 4-7.) The amended feature of claim 1, in comparison, recites adding an instruction during translation that will branch to correction code to adjust the stack during the time of execution. The instruction operates during execution of the instructions, and as such, the instruction will branch to the correction code to adjust the stack during execution. Therefore, translation

does not have to restart as the stack will be adjusted during execution. This is not the same as rolling back execution to the beginning of the translation to adjust the stack, and then restarting translation from the beginning. Therefore, claim 1 is patentable over Rozas.

Claims 4, 5, 16, and 19 depend from claim 1 and include additional limitations. Therefore, claims 4, 5, 16, and 19 are also patentable over Rozas.

Independent claims 6 and 11 also recite, in part, adding an instruction during translation, the instruction branches to correction code if said expected TOS is not equal to said actual TOS, and wherein said correction code to adjust said stack for said first block of instructions at the time of executing said translated first block of instructions. As discussed above, Rozas does not disclose or suggest such a feature. As a result, claims 6 and 11 are patentable over Rozas for the reasons discussed above with respect to claim 1. Claims 9, 10, and 14-21 variously depend from claims 6 and 11, and include additional limitations. Therefore, claims 9, 10, and 14-21 are also patentable over Rozas.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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